

L Number	Hits	Search Text	DB	Time stamp
3	3	((("6025267") or ("6013943") or ("6004829"))).PN.	USPAT; US-PGPUB	2004/08/26 16:38
4	5	((("6057220") or ("6020024") or ("6015730") or ("6007671") or ("6004843"))).PN.	USPAT; US-PGPUB	2004/08/26 16:39
5	86	(protect or protecting) with (FOX or (filed adj oxide) or (buried adj oxide))	USPAT; US-PGPUB	2004/08/26 16:45
6	2	((protect or protecting) with (FOX or (filed adj oxide) or (buried adj oxide))) and (clean\$3 with substrate)	USPAT; US-PGPUB	2004/08/26 16:43
7	207	(cover or covering) with (FOX or (filed adj oxide) or (buried adj oxide))	USPAT; US-PGPUB	2004/08/26 16:46
8	7	((cover or covering) with (FOX or (filed adj oxide) or (buried adj oxide))) and (clean\$3 with substrate)	USPAT; US-PGPUB	2004/08/26 16:43
9	16	(protect or protecting) with (FOX or (filed adj oxide) or (buried adj oxide))	EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:45
10	42	(cover or covering) with (FOX or (filed adj oxide) or (buried adj oxide))	EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:46

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TITLE: Formation of bipolar transistor
having emitter, base, and collector, comprises doping mask
covering bird's beak formed between filed oxide layers and
doped regions of substrate, and adding silicide layer
to exposed surface of doped regions

----- KWIC -----

Title - TIX (1):

Formation of bipolar transistor having emitter, base,
and collector, comprises doping mask covering bird's beak formed between
filed oxide layers and doped regions of substrate, and adding silicide layer
to exposed surface of doped regions

US-PAT-NO: 5780331

DOCUMENT-IDENTIFIER: US 5780331 A

TITLE: Method of making buried contact
structure for a MOSFET
device in an SRAM cell

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Detailed Description Text - DETX (7):

After removal of photoresist shapes, 8a, and 8b, using plasma oxygen ashing and careful wet cleans, a lightly doped source and drain region, 9, is formed in regions of semiconductor substrate, 1, not covered by FOX regions, 2, not covered by polycide gate structure, 20, and not covered by buried contact structure, 21. The lightly doped source and drain region is formed via ion implantation of arsenic or phosphorous, at an energy between about 25 to 75 KeV, at a dose between about $7E13$ to $7E14$ atoms/cm.^{sup.2}. A layer of silicon oxide is next deposited using either LPCVD or plasma enhanced chemical vapor deposition, (PECVD), procedures, at a temperature between about 500.degree. to 700.degree. C., to a thickness between about 1000 to 3000 Angstroms, using tetraethylorthosilicate, (TEOS), as a source. An anisotropic RIE procedure, using CHF.sub.3 as an etchant, is used to create silicon oxide spacers, 10, on the sides of the polycide gate structure, 20, as well as on the sides of buried contact structure, 21, schematically shown in FIG. 5. Also shown in FIG. 5, is the creation of a heavily doped source and drain region, 11, formed in regions of semiconductor substrate, 1, not covered by FOX regions, 2, not by polycide gate structure, 20, or buried contact structure, 21, and

not covered by silicon oxide spacers, 10. The heavily doped source and drain region, 11, obtained via ion implantation of either arsenic or phosphorous, at an energy between about 30 to 100 KeV, at a dose between about $1E15$ to $6E15$ atoms/cm.², produces a conductive link between the buried contact region, 6b, and the gate region underlying polycide gate structure, 20. If thin tab of tungsten silicide, 7c, was not present during the patterning of the buried contact structure, 21, and the polycide gate structure, 20, trenching or crevicing at the edge of the buried contact structure may have occurred, making it difficult to form a heavily doped source and drain region, via ion implantation procedures, in the trenched region, resulting a decreased link-up to the buried contact region.

Claims Text - CLTX (11):

a second anisotropic etching procedure, removing bottom portion of said split polysilicon shape, in an area not covered by said first photoresist shape, to create said polycide gate structure, on underlying gate insulator layer, while removing bottom portion of said split polysilicon shape, on said FOX region, in an area not covered by said second section of said second photoresist shape, creating said buried contact structure, with thin metal silicide tab protecting underlying region of buried contact region from said second anisotropic RIE procedure, in an area not covered by said first section of said second photoresist shape;

US-PAT-NO: 5744391

DOCUMENT-IDENTIFIER: US 5744391 A

TITLE: Method to improve isolation between
EEPROM devices via a field oxide anneal

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Brief Summary Text - BSTX (6):

A major feature of a EEPROM device is a tunnel insulator layer, which allows the cell to be programmed and erased via Fowler-Nordheim tunneling. Field oxide, (FOX), regions are used for physical and electrical isolation between EEPROM cells, or between specific devices in an EEPROM cell. However specific processing steps, such as a tunnel ion implantation procedure, result in implanting dopants entering the FOX layer, and increasing the etch rate of the FOX layer, in hydrofluoric, (HF), containing wet etchants. Since wet etchants are used in the fabrication sequence of EEPROM devices, a initially thick, FOX region, can be significantly thinned as a result of subsection to wet clean treatments, containing HF. The thinning of the FOX region, and subsequent decrease in isolation between EEPROM cells, or devices, can result in deleterious device parameters. This invention will teach a process for fabricating semiconductor device cells, such as EEPROM cells, consisting of tunnel transistors, separated by a FOX region, in which the thinning of the FOX region via subsection to wet treatments, incorporating HF, is minimized by the addition of a post-tunnel implant anneal procedure. Prior art, such as Roberts, in U.S. Pat. No. 5,376,577, describes a process

for forming a static random access memory, (SRAM), device, in which the **FOX** region is subjected to an ion implantation procedure, followed by the growth of a sacrificial oxide layer on the **FOX** region, performed to protect the implanted **FOX** region from subsequent wet etch treatments. However the addition of a sacrificial oxide would not be desirable to an EEPROM process, and therefore the post-tunnel implant, anneal procedure, is the preferred procedure for the EEPROM process.

Detailed Description Text - DETX (3):

FIG. 1, shows the early stages of processing, used to fabricate N type, tunnel transistors, of an EEPROM cell, separated by FOX regions, 3a. A P type, silicon substrate, 1, with a $\langle 100 \rangle$ crystallographic orientation is used. P well regions, 2, are formed in areas to subsequently contain for N type, tunnel transistors, via photolithographic blockout procedures, allowing an ion implantation of B.sup.1 to be performed at an energy between about 70 to 110 KeV, at a dose between about $8E11$ to $2E13$ atoms/cm.sup.2, in areas not blocked by photoresist. After removal of photoresist via plasma oxygen ashing and careful wet cleans, a composite insulator layer, consisting of a thermally grown, underlying silicon dioxide layer, and an overlying silicon nitride layer, deposited using either low pressure chemical vapor deposition, (LPCVD), or plasma enhanced chemical vapor deposition, is formed on the silicon substrate, 1. A photoresist shape, is used as a mask to create an oxidation resistant, composite insulator shape, in the silicon nitride - silicon dioxide layers, via an reactive ion etching procedures, using CHF.sub.3 as an etchant. After removal of the photoresist shape, using plasma oxygen ashing and careful

wet cleans, the oxidation resistant, composite insulator shape is used as a mask to allow a FOX region, 3a, to be thermally grown in unmasked regions of silicon substrate, 1. Fox regions, 3b, are thermally grown in an oxygen-steam ambient, at a temperature between about 850.degree. to 1050.degree., to an initial thickness, between about 4800 to 5200 Angstroms. The oxidation resistant, composite insulator shape, is removed, using hot phosphoric acid for the overlying silicon nitride layer, and a buffered HF solution for the underlying silicon dioxide layer, resulting in the structure shown schematically in FIG. 1.